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H4F
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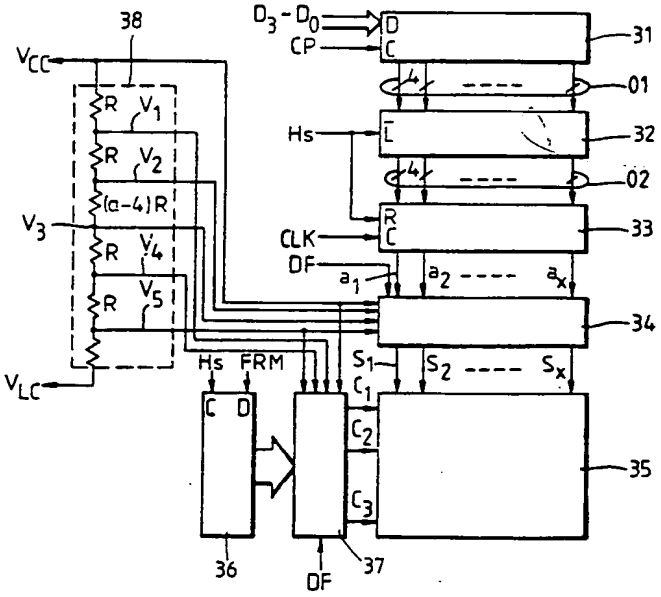
G09F G09G H04N

(54) Electro-optical modulator

(57) In an electro-optical modulator suitable for use in display devices or as an optical shutter array in a printer and including a dot matrix LCD panel 35 using supertwisted birefringence effect, the signal electrode driver enables grey scale variations to be produced at selected LC cells. Either the pulse width or the frequency of the signals applied to the signal electrodes may be made dependent on the grey scale data D_3-D_0. The signal driver may include a shift register 31, a latch 32 and a grey scale control circuit 33 which controls the pulse width in dependence upon the period of a grey scale clock CLK. For obtaining optimum grey scale characteristics that matches the reflectivity characteristics of the LC device either the period of the grey scale clock CLK may be adjusted or a suitable code - conversion circuit may be provided before the shift-register 31. Circuits 37, 34 control the voltage levels of the scan, data pulses.

Fig.3.



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The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.

Fig.1.

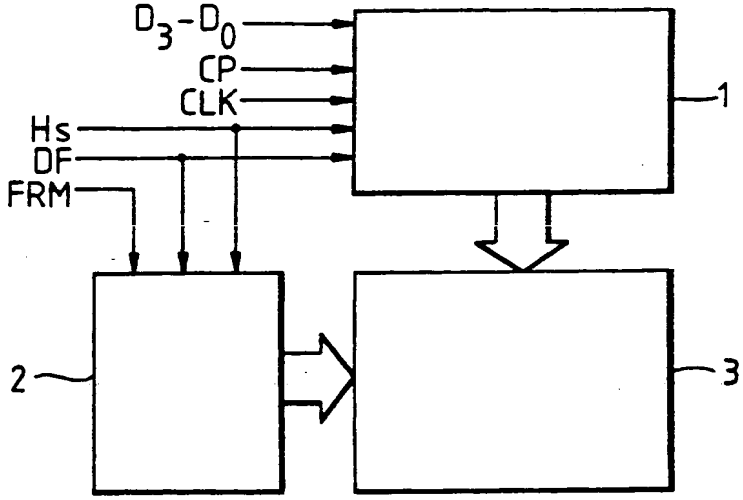

Fig.2.

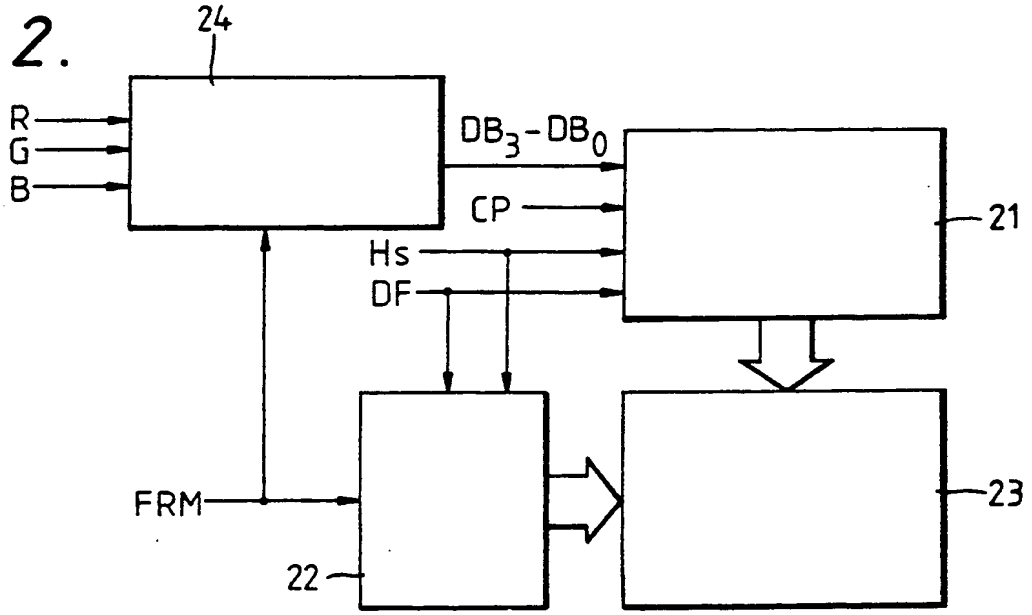

Fig.13.

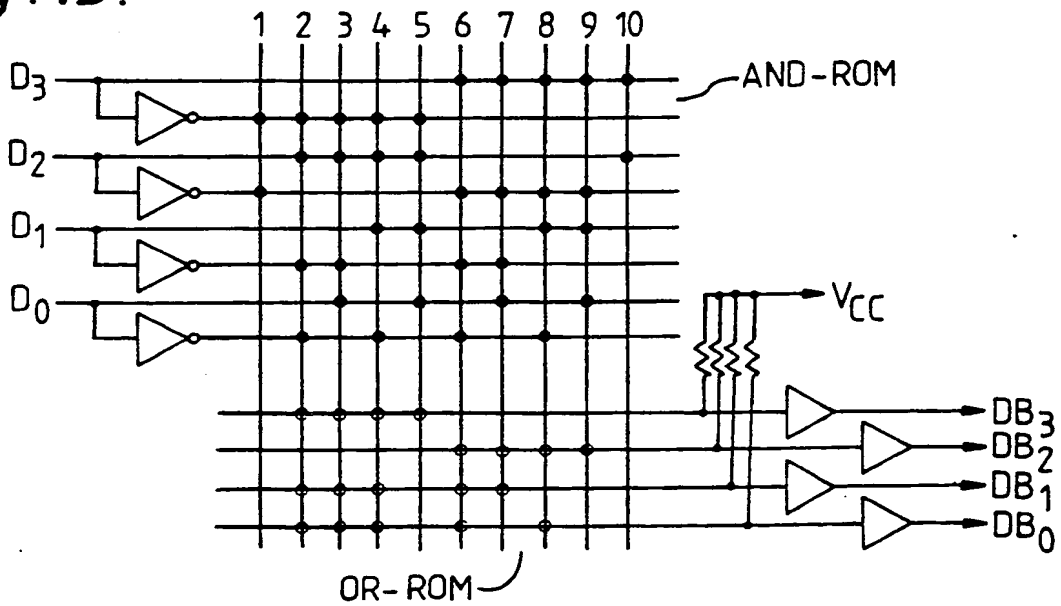

Fig.3.

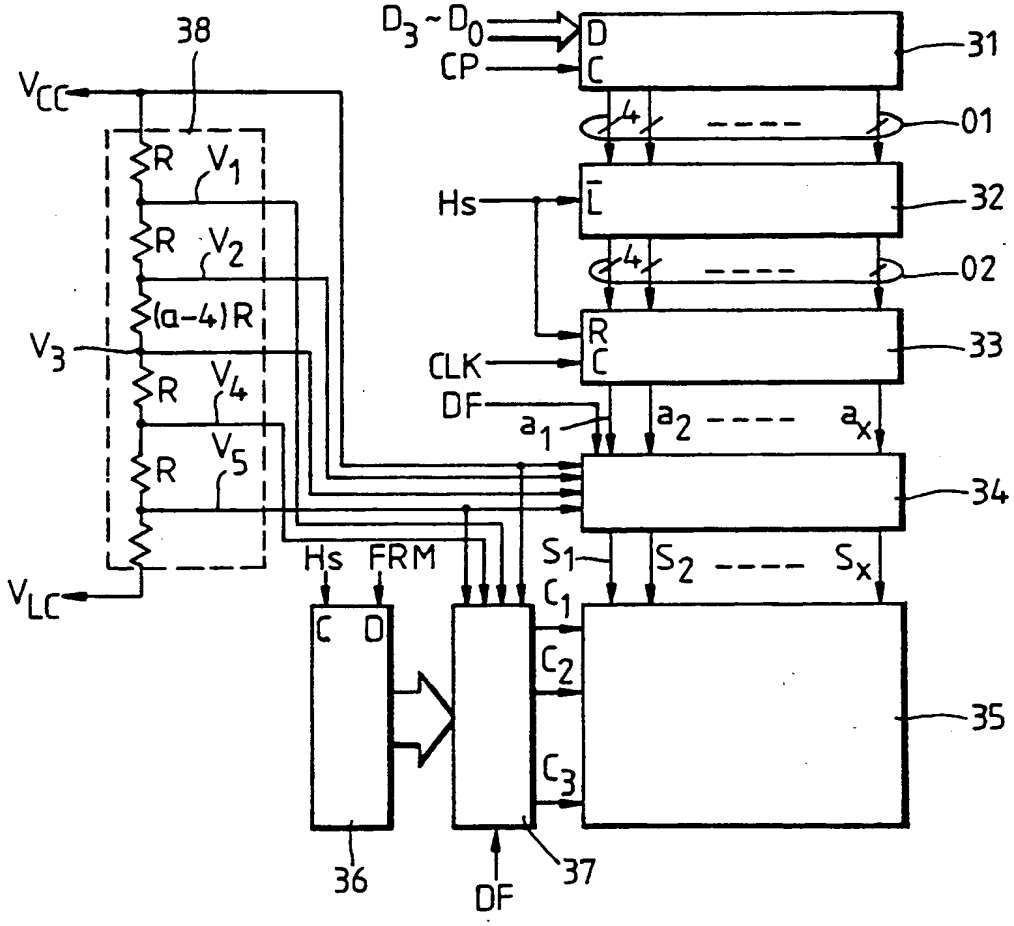

Fig. 4.

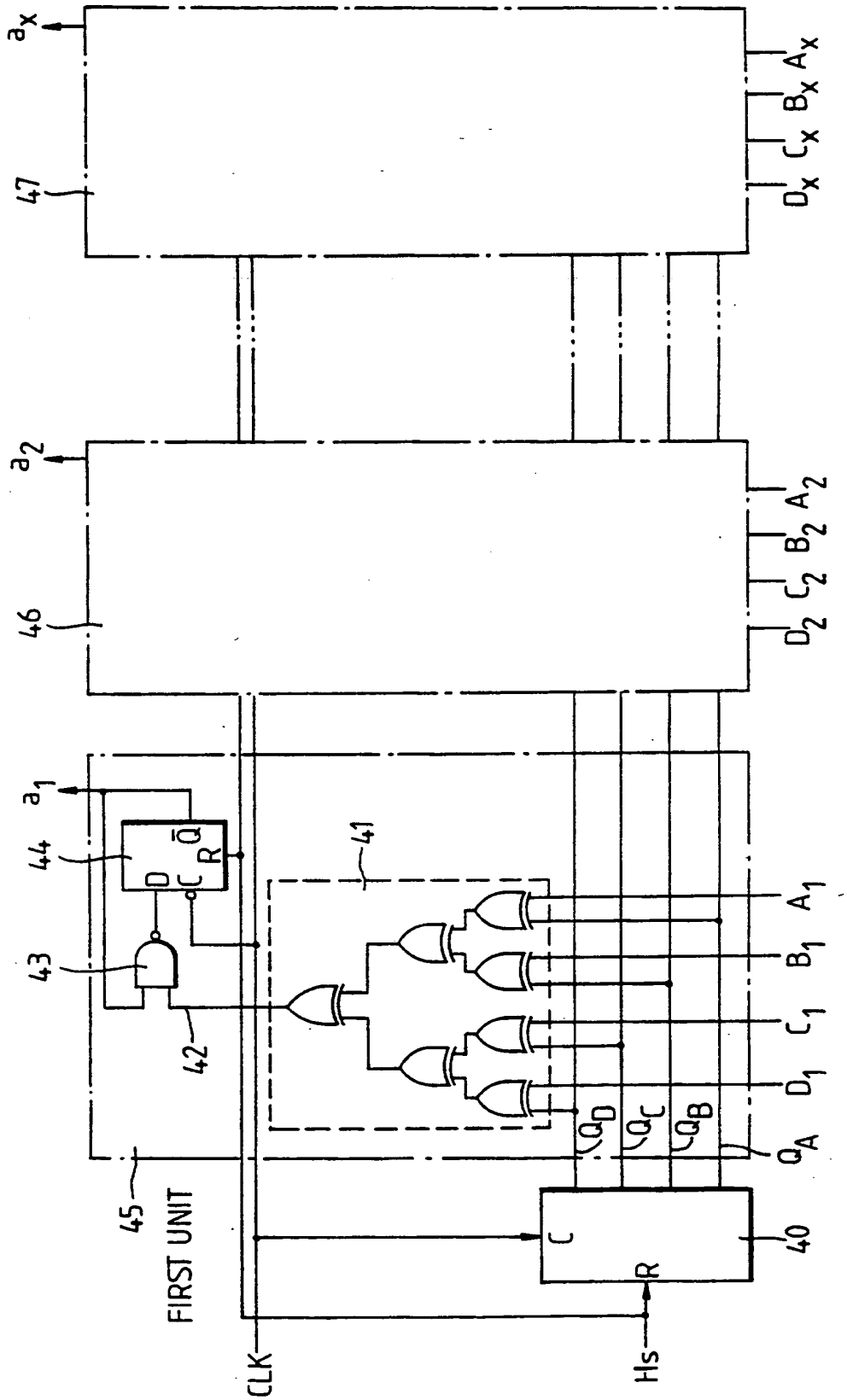

Fig. 5.

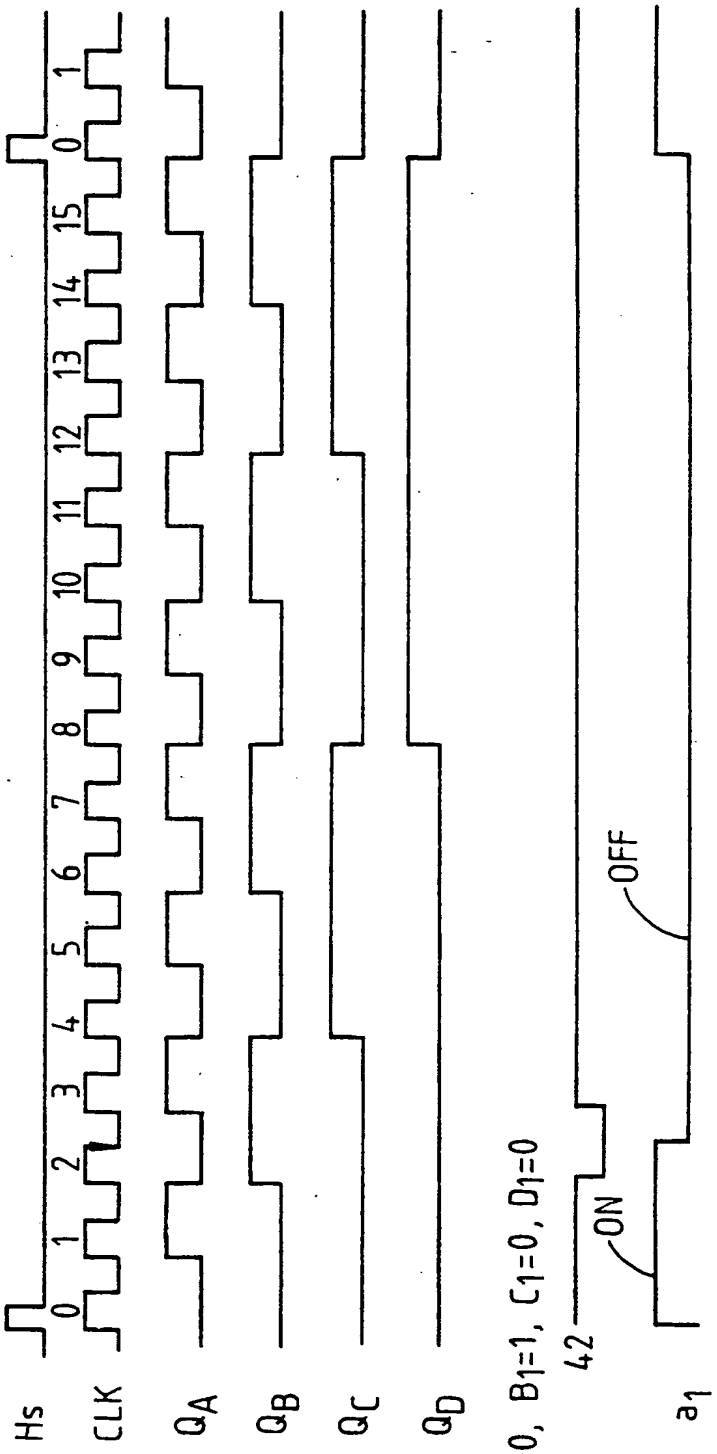

Fig. 6.

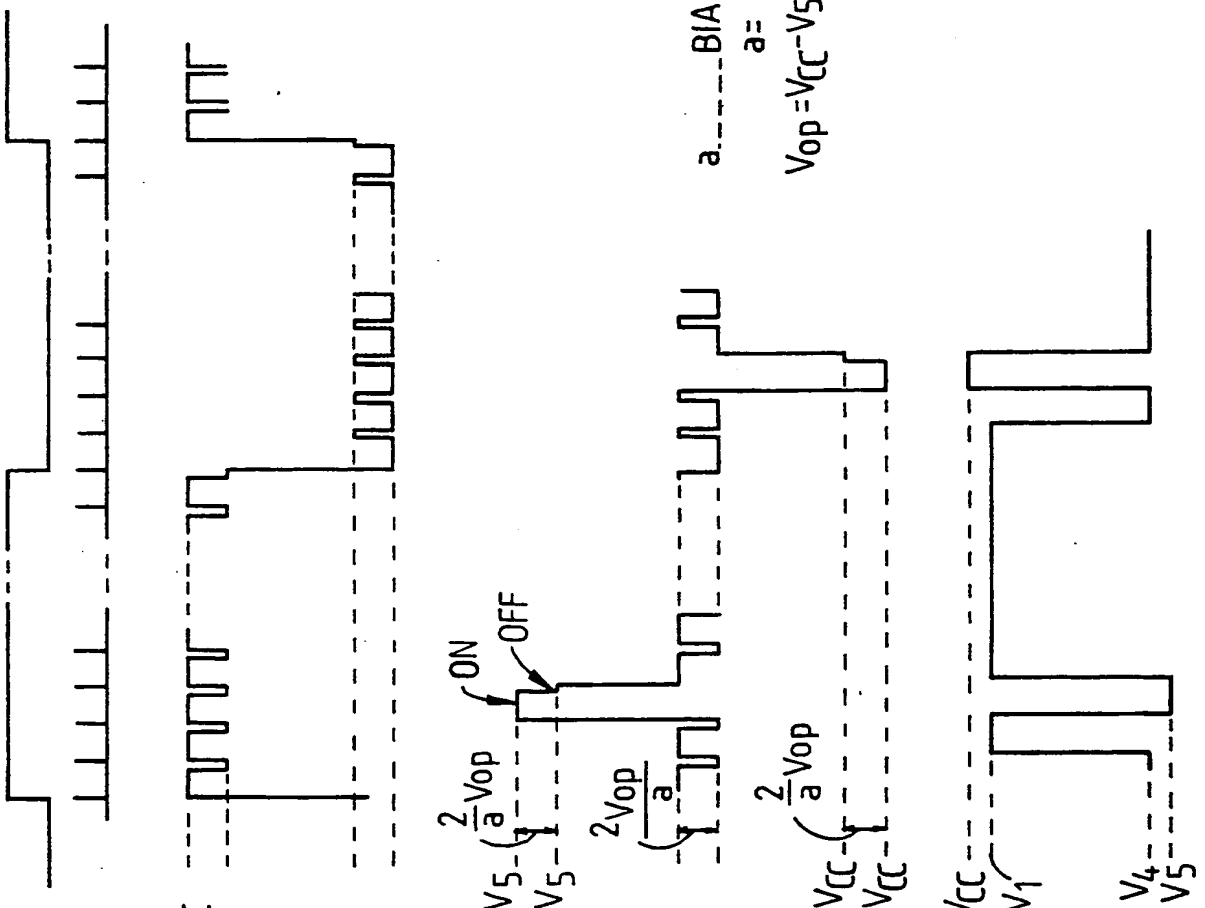

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Fig.7.

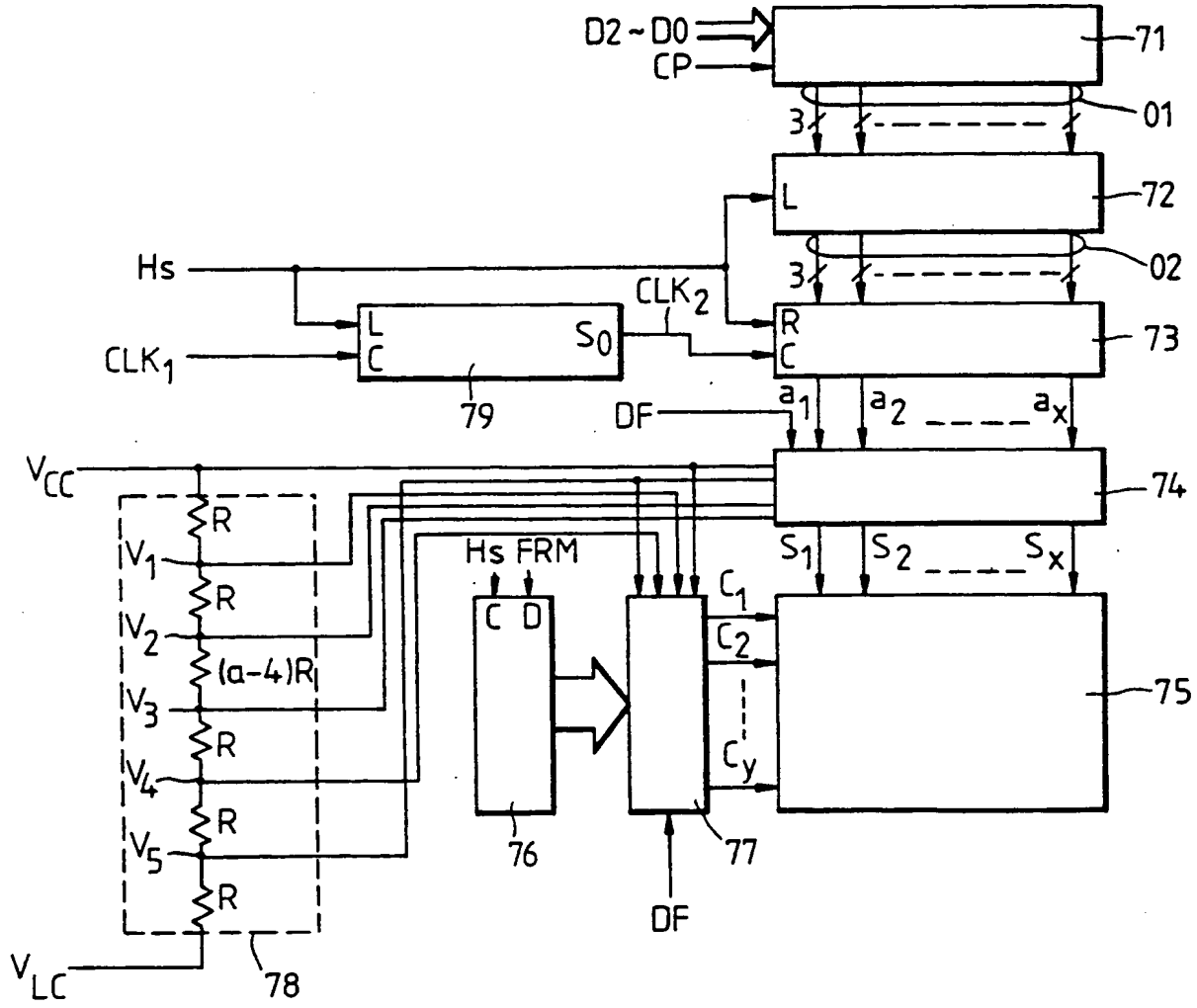

Fig. 8.

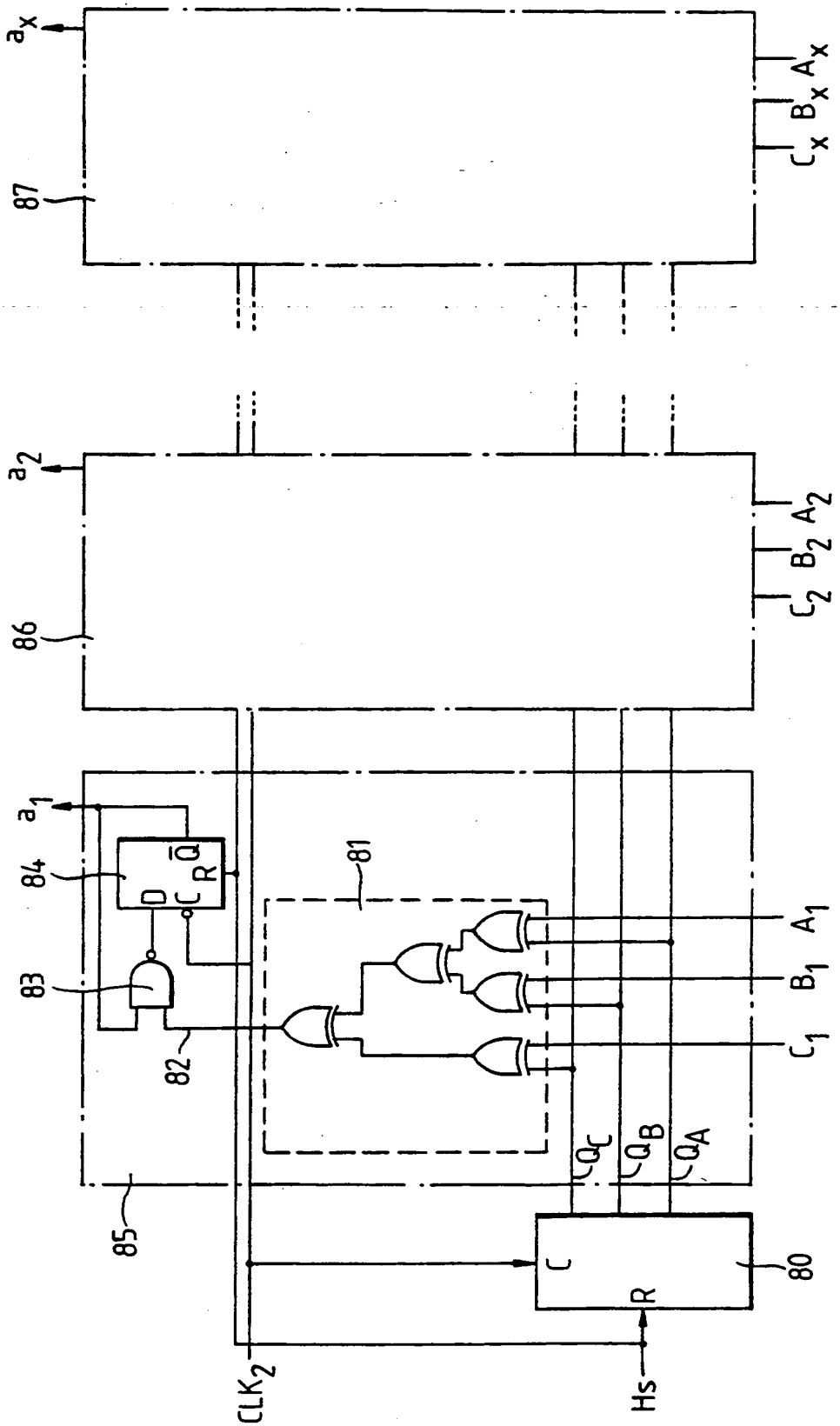

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Fig. 9.

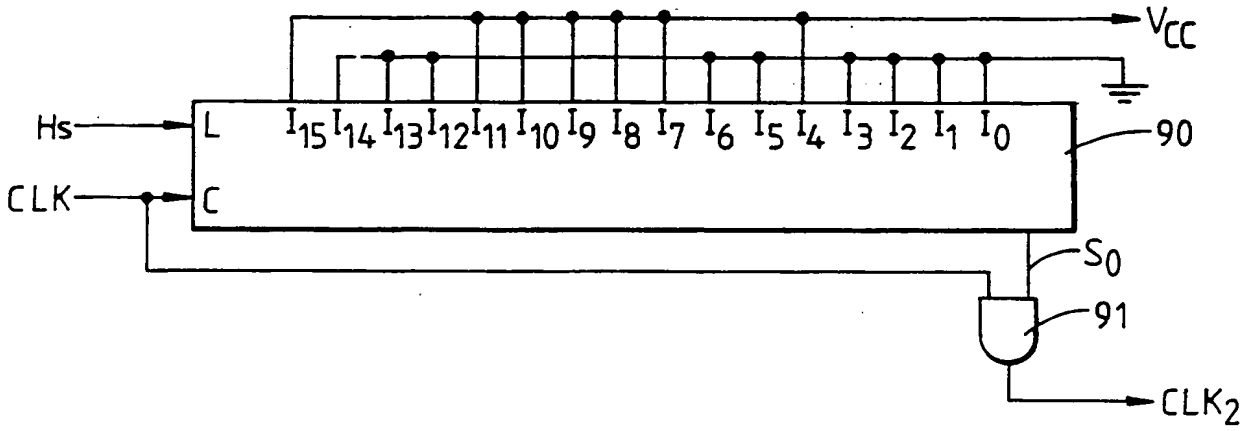

Fig. 10.

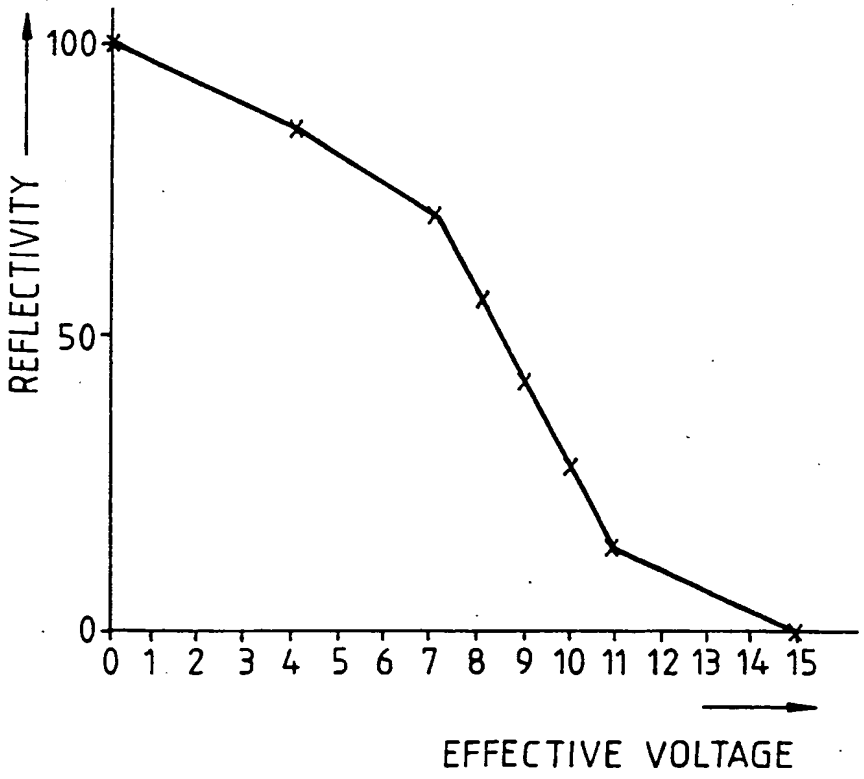

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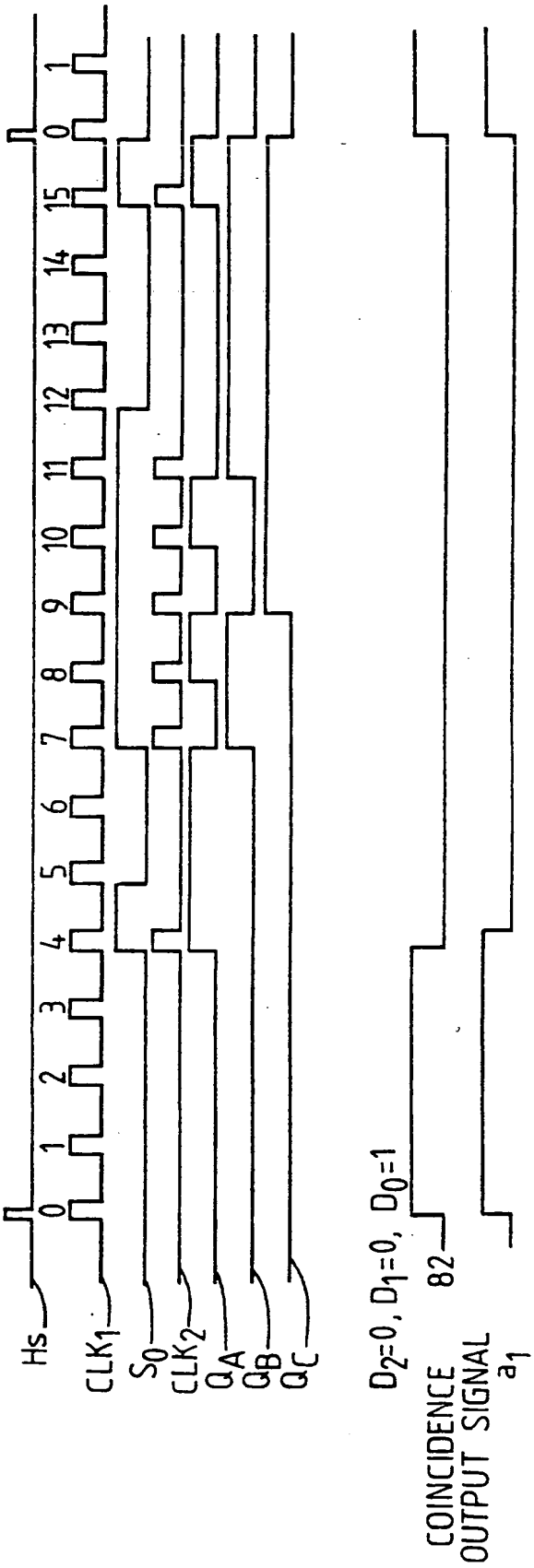
Fig. 11.



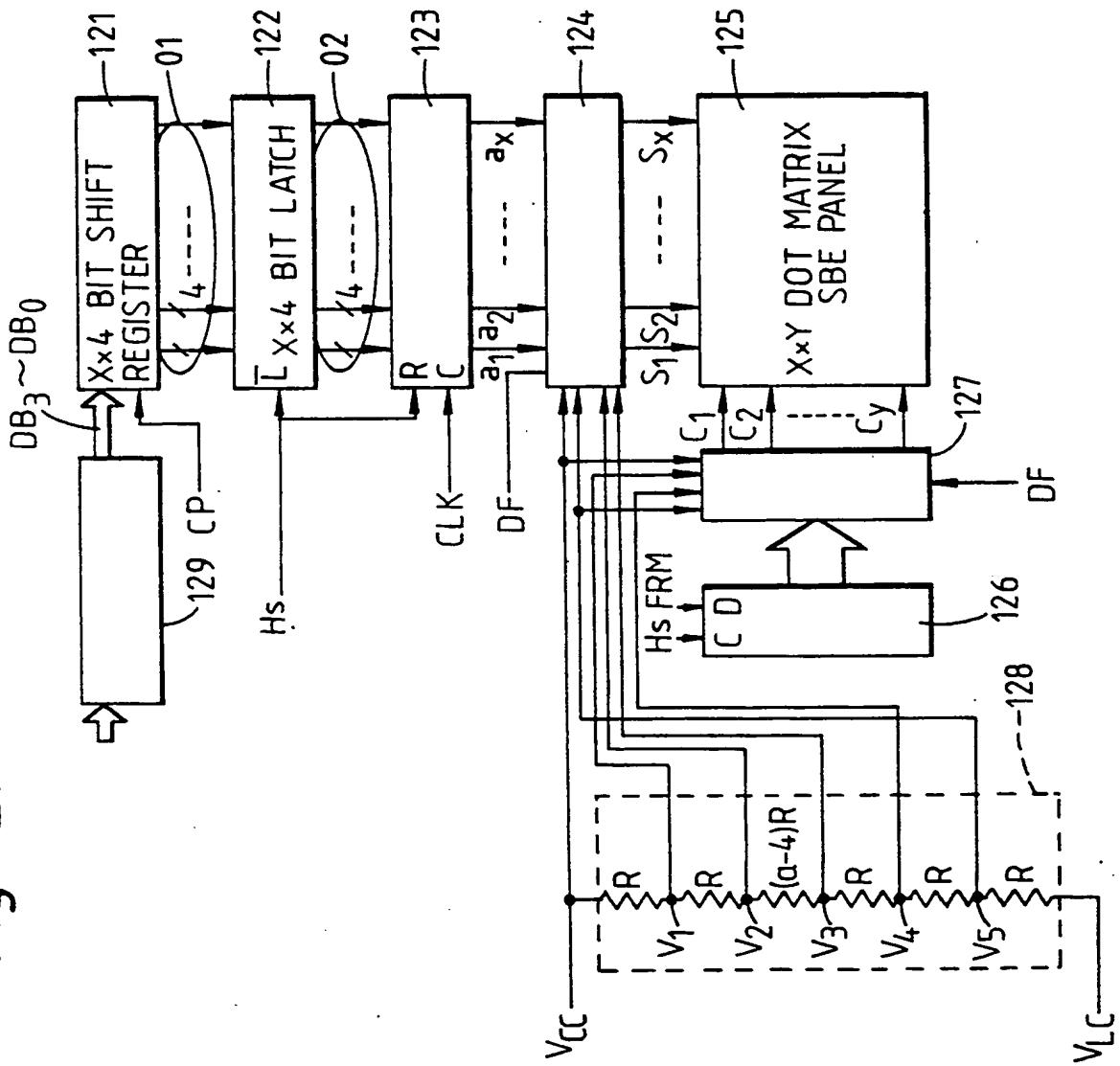
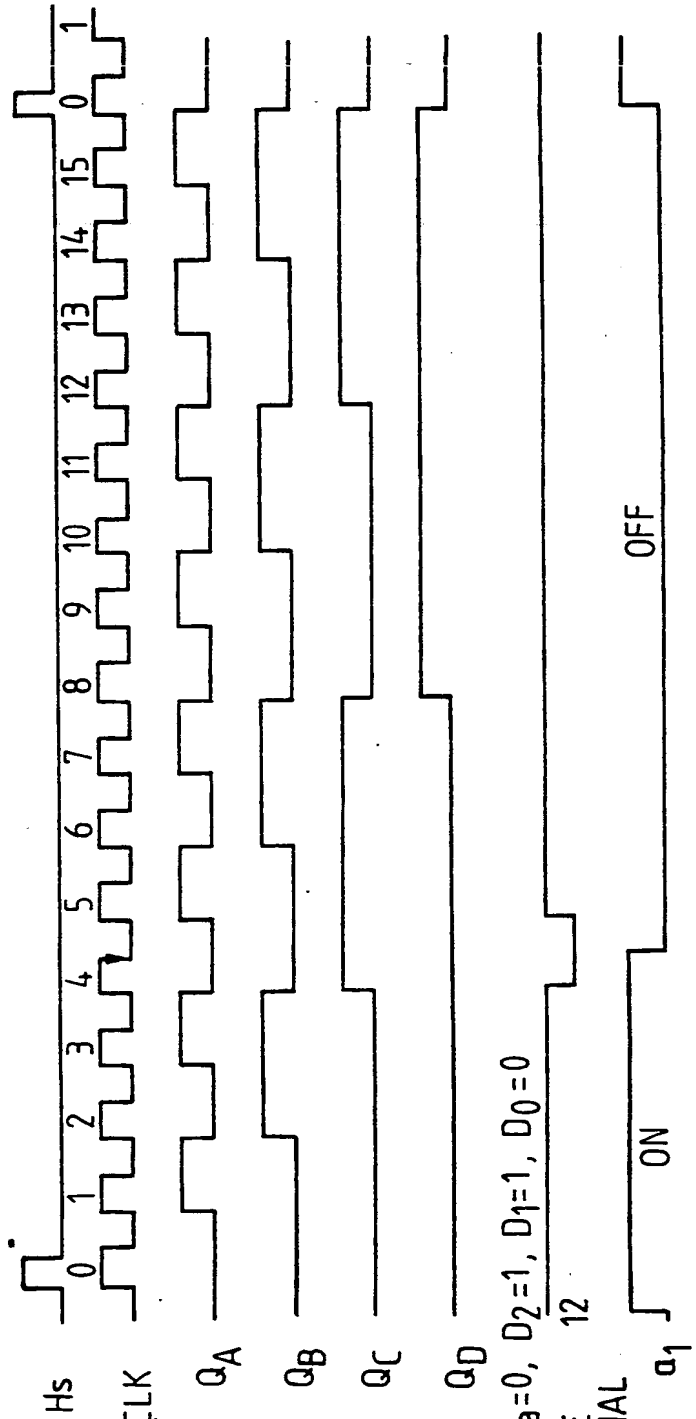


Fig. 12.

Fig. 14.



ELECTRO-OPTICAL MODULATOR

This invention relates to electro-optical modulators, for example, display devices, optical shutter arrays, etc. and more particularly to liquid crystal devices using the supertwisted birefringence effect (SBE).

A so-called SBE-type liquid crystal electro-optical modulator which has a twist angle of 180° to 360° and utilises birefringence effect is known from Japanese Patent Publication No. 107020/1985 (U.S. Patent No. 4634229). However, there has not hitherto been proposed a device in which SBE cells arranged in the form of a dot matrix are driven by pulse-width modulation to realise a grey scale display.

The present invention seeks to provide an electro-optical modulator with means for obtaining optimum grey scale characteristics that meet reflectivity characteristics of SBE cells.

Although the present invention is primarily directed to any novel interger or step, or combinationof integers or steps, herein disclosed and/or as shown in the accompanying drawings, nevertheless according to one particular aspect of the present invention to which, however the invention is in no way restricted, there is provided an electro-optical modulator comprising: a dot matrix liquid crystal panel (3) using supertwisted birefringence effect, the panel having a plurality of scanning electrodes and a plurality of signal electrodes; a scanning electrode driving means; and a signal electrode driving means having a grey scale function.

The grey scale function may be, in operation, performed by frequency modulation.

Alternatively, the grey scale function may be, in operation, performed by pulse width modulation. The signal electrode driving means preferably includes means for changing grey scale display data to a signal with a desired pulse width to be applied to the signal electrodes.

In operation, the grey scale display data may be changed to a signal with a desired pulse width which has one or more units, one unit being equal to a period of a grey scale control clock.

The electro-optical modulator may have a plurality of grades of grey scale function, each pulse width corresponding to each of the grades of the grey scale being set so that the change of the grades of grey scale to the change of the grades of the pulse width is substantially constant. In operation, the pulse width may be changed by changing the period of the grey scale control clock signal.

In one embodiment the signal electrode driving means comprises a shift register for receiving and shifting grey scale data, a latch for latching the output of the shift register, a grey scale controller for changing the output of the latch to a signal having a desired selective time width according to the content of the output of the latch, the desired selective time width having one or more units one of which is equal to a period of a grey scale control clock, and a signal electrode driver for changing the output of the grey scale controller to a liquid crystal driving signal. Thus, the grey scale controller may comprise a counter for counting the grey scale control clock, and a plurality of circuit units each of which has a

coincidence circuit for examining coincidence between the output signal of said counter and the output signal of the latch, and a latching circuit for latching the output of the coincidence circuit synchronising with the grey scale control clock.

The number of circuit units is preferably equal to that of signal electrodes of the panel.

The grey scale display data may be 2, 3 or 4 bits.

In another embodiment the electro-optical modulator includes a code conversion circuit for converting grey scale data to codes so as to obtain optimum grey scale.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of one embodiment of an electro-optical modulator according to the present invention;

Figure 2 is a block diagram of another embodiment of an electro-optical modulator according to the present invention;

Figure 3 is a block diagram of a further embodiment of an electro-optical modulator according to the present invention;

Figure 4 is a diagram which shows a grey scale controller of the electro-optical modulator of Figure 3 in detail;

Figure 5 is a time chart illustrating operation of the grey scale controller of Figure 4;

Figure 6 is a diagram of waveforms for driving an SBE panel;

Figure 7 is a block diagram which illustrates a fourth embodiment of an electro-optical modulator according to the present invention;

Figure 8 is a diagram which shows a grey scale

controller of the electro-optical modulator of Figure 7 in detail;

Figure 9 is a diagram which shows a grey scale control clock circuit of the electro-optical modulator of Figure 7;

Figure 10 is a diagram showing the relationship between reflectivity of an SBE panel and effective voltage;

Figure 11 is a time chart illustrating the operation of the grey scale controller of Figure 8;

Figure 12 is a block diagram of another embodiment of electro-optical modulator according to the present invention;

Figure 13 is a diagram illustrating code conversion in the electro-optical modulator of Figure 12; and

Figure 14 is a time chart of a grey scale controller of the electro-optical modulator of Figure 12.

Figure 1 illustrates one embodiment of an electro-optical modulator according to the present invention. The electro-optical modulator comprises a signal electrode driver 1 having a grey scale (gradation) function, a scanning electrode driver 2 and a dot matrix liquid crystal (LC) panel 3 using the super-twisted birefringence effect (SBE).

Grey scale display data D_3 to D_0 for one line are input to the signal electrode driver 1 synchronising with the shift clock CP every horizontal synchronising signal Hs and is latched therein. The input grey scale display data D_3 to D_0 is compared with the number of grey scale control clocks CLK and is converted to a signal with a desired pulse width which has one or more units each of which is equal to the period of the grey

scale control clock CLK. The selected pulse width makes a signal electrode line of the dot matrix LC panel 3 change to the selected state. The horizontal synchronising signal Hs selects scanning electrode lines of the scanning electrode driver 2 in sequence. Scanning of the scanning electrode lines is started in accordance with a frame signal FRM generated every frame as a trigger. DF is a LC AC signal.

Grey scale display data D_3 to D_0 may be changed to a desired signal for grey scale display not only by pulse width modulation as shown in Figure 1, but also by frequency modulation as shown in Figure 2. In Figure 2 another embodiment of an electro-optical modulator according to the present invention has a signal electrode driver 21 having a grey scale function and a frequency modulation circuit 24. Pixel data R,G,B including grey scale display information are frequency-modulated by the frequency modulation circuit 24 every frame signal and is changed to grey scale display data DB_3 to DB_0.

Grey scale display data DB_3 to DB_0 for one line is input to the signal electrode driver 21 synchronising with the shift clock CP every horizontal synchronising signal Hs and is latched therein. The grey scale display data DB_3 to DB_0 makes a signal electrode line of a dot matrix liquid crystal (LC) panel 23 change to a selected or a non-selected state according to "high" or "low" states of the grey scale display data. The horizontal synchronising signal Hs selects the scanning electrode line of a scanning electrode driver 22 and is started in accordance with a frame signal FRM generated every frame as a trigger.

Figure 3 illustrates a further embodiment of an electro-optical modulator according to the present

invention. In Figure 3, supertwisted birefringence effect cells 35 (hereinafter referred to as SBE cells) arranged in the form of an X x Y dot matrix (where X denotes horizontal dots and Y denotes vertical dots) are driven by 4-bit grey scale data to modulate the pulse time width into 16 grey scales to produce the display.

4-bit grey scale data D_3 to D_0 is shifted in an X x 4 bit shift register 31 by the shift clock CP. An output 01 of the shift register 31 is latched by an X x 4 bit latch 32 that has X x 4 bit structure when a horizontal synchronising signal Hs also fed thereto falls. An output 02 of the latch 32 serves as an input signal to a grey scale controller 33.

Figure 4 illustrates in detail the grey scale controller 33 which consists of a plurality (x) of circuit units 45,46,47 to correspond to horizontal dots. Each unit has the same circuit structure and, hence, only the first unit 45 will be described. A re-set terminal R of a 4-bit binary counter 40 performs an active high operation and is connected to receive a horizontal synchronising signal Hs. A terminal C is a clock terminal connected to receive the grey scale control clock CLK. The time chart of Figure 5 illustrates the relationship between the horizontal synchronising signal Hs and the grey scale control clock CLK. That is, 16 grey scale control clocks CLK are input within one period of the horizontal synchronsing signal Hs with the rise thereof as a starting point.

The binary counter 40 of Figure 4 is cleared by the horizontal synchronising signal Hs of high level, and then performs a binary counting operation in response to the rise of the grey scale control clock CLK. Symbols Q_A, Q_B, Q_C, Q_D denote output signals of 2^0, 2^1, 2^2, 2^3 respectively of the binary counter 40.

A coincidence circuit 41 of the first unit 45 examines the coincidence between the output signals Q_A, Q_B, Q_C, Q_D of the binary counter 40 and signals A_1, B_1, C_1, D_1. The signals A_1, B_1, C_1, D_1 are output signals 2^0, 2^1, 2^2, 2^3 of the latch 32.

A coincidence output signal 42 assumes a low level when the output signals Q_A, Q_B, Q_C, Q_D of the binary counter 40 become equal to the output signals A_1, B_1, C_1, D_1 of the latch 32. The coincidence signal 42 causes a data terminal D of a D-type flip-flop 44 to assume high level via a NAND gate 43. Since the grey scale control clock CLK is connected to the clock terminal C of the flip-flop 44, an output signal a_1 of the first unit 45 which is produced by the flip-flop 44, assumes low level in response to fall of one grey scale control clock CLK. The output signal a_1 of the first unit is connected to one input of the NAND gate 43 and, hence, maintains low level even when the level of the coincidence output signal 42 is returned to high level. Thereafter, the flip-flop 44 is cleared by the horizontal synchronising signal Hs, and the output signal a_1 of the first unit assumes high level. At the same time, the binary counter 40 is re-set. During the period in which the output signal a_1 of the first unit assumes high level, a selective waveform is applied to the panel 35 through an X bit signal electrode driver 34 shown in Figure 3. The time chart of Figure 5 illustrates the operation of the grey scale controller 33 in the case where the 4-bit grey scale data is as follows:

$D_3 = 0$ ....MSB
$D_2 = 0$
$D_1 = 1$
$D_0 = 0$

0 .... low level
1 .... high level

In this case, the first stage of the latch 32 produces an output:

$D_1 = 0$
$C_1 = 0$
$B_1 = 1$
$A_1 = 0$

whereby the coincidence output signal 42 assumes high level at the moment when the grey scale control clock CLK is 0, and assumes low level at the moment when the grey scale control clock CLK is 2. The output signal a_1 of the grey scale controller 33 assumes low level at a moment when the grey scale control clock-2 falls, and this condition is maintained until the next horizontal synchronising signal Hs is input.

The period in which the output signal a_1 of the first unit of the grey scale controller 33 assumes high level is about 2/16 of the period of the horizontal synchronising signal Hs, and the period of high level changes depending upon the 4-bit grey scale data D_3 to D_0.

The output signals a_1 to a_x of the grey scale controller 33 drive signal electrodes S_1 to S_x of the panel 35 through the signal electrode driver 34 of Figure 3. Electrodes C_1 to C_y of the scanning side of the panel are driven by a voltage averaging method that is usually employed for driving liquid crystal cells, by a Y bit shift register 36 and a Y bit scanning electrode driver 37. A signal FRM is a frame signal which

indicates the start of a frame, and DF denotes a liquid crystal AC inverting signal.

A power supply 38 generates a selective voltage or a non-selective voltage that is applied to the signal electrode driver 34 and to the scanning electrode driver 37.

Figure 6 illustrates a drive waveform that is applied to the panel 35, wherein the ON portion in the voltage corresponds to the ON portion of the output signal a_1 in the time chart of Figure 5.

As described above, the SBE cells of the panel 35 are arranged in the form of a dot matrix and are grey scale-driven by pulse-width modulation in order to display relatively large amounts of data maintaining a high display quality.

Figure 7 illustrates another embodiment of an electro-optical modulator according to the present invention. In the embodiment of Figures 7, SBE cells arranged in the form of an X x Y dot matrix SBE panel 75 are driven by 3-bit grey scale data to modulate the pulse time width into 8 grey scales to realise the display.

3-bit grey scale data D_2 to D_0 are shifted in an X x 3-bit shift register 71 by a shift clock CP. The output 01 of the shift register 71 is latched by an X x 3-bit latch 72 that has X x 3-bit structure, when a horizontal synchronising signal Hs falls. Output 02 of the latch 72 serves as an input signal to a grey scale controller 73.

Figure 8 illustrates in detail the grey scale controller 73, and Figure 9 illustrates in detail the grey scale control clock circuit 79.

The grey scale control clock circuit 79 generates from a first grey scale control clock CLK1 a second grey

scale control clock CLK2 which determines the width of a grey scale pulse. The period of the second grey scale control clock CLK2 determines the selective time width that will be applied to the panel 75 as will be described later.

As shown in Figure 10, the relationship between the reflectivity of an SBE panel and the effective voltage is not linear, i.e. the gradient changes at each point of the effective voltage. To obtain the optimum grey scale display, therefore, the reflectivity must be changed depending upon the grey scale data such that the gradient of refractive index is uniform at each of the effective voltages.

Figure 10 shows the relationship between the reflectivity of the SBE panel and the effective voltage, where the grey scale has 8 grades so that the reflectivity uniformly changes over a range from 100% to 0% of reflectivity.

As shown in Figure 9, the first grey scale control clock CLK1 serves as a shift clock for a 16-bit parallel input shift register 90 of the grey scale control clock circuit 79 which has parallel input terminals I_0 to I_{15} of 16-bits. The data of these parallel input terminals is determined by a relation between the reflectivity of the panel 75 and the effective voltage shown in Figure 10. The reflectivity drops by 1/7 of 100% from a moment at which the effective voltage is 0 to a moment at which the effective voltage is 4. That is, a low level is input to parallel input terminals I_0 to I_3 of the shift register 90, and a high level is input to the input terminal I_4.

Data is input in parallel to the input terminals I_0 to I_{15} in response to a horizontal synchronising signal Hs of high level. After the horizontal

synchronising signal Hs has returned to low level, the data is shifted by the first grey scale control clock CLK1 and is produced through a serial output signal S_0, thereby, forming the second grey scale control clock CLK2 via an AND gate 91.

The second grey scale control CLK2 is sent to the grey scale controller 73 of Figure 8. The grey scale controller 73 consists of a plurality (x) of circuit units 85,86,87 to correspond to X horizontal dots. Each unit has the same circuit structure. Therefore, only the first unit 85 will be described. A re-set terminal R of a 3-bit binary counter 80 performs an active high operation and is connected to receive a horizontal synchronising signal Hs. A terminal C is a clock terminal connected to receive the second grey scale control clock CLK2. Figure 11 is a time chart illustrating the relationship between the horizontal synchronising signal Hs and the second grey scale control clock CLK2. In one period of the horizontal synchronising signal Hs, there are input 16 first grey scale control clocks starting from a moment at which the horizontal synchronising signal rises.

The binary counter 80 is cleared by the horizontal synchronising signal Hs of high level, and performs a binary counting operation in response to a rise of the second grey scale contol clock CLK2.

A coincidence circuit 81 examines coincidence of output signals Q_A, Q_B, Q_C of the binary counter 80 and signals A_1, B_1, C_1 of the latch 72. Signals Q_A, Q_B, Q_C denote output signals of 2^0, 2^1 and 2^2 respectively of the binary counter 80 and signals A_1, B_1, C_1 denote output signals of 2^0, 2^1, 2^2 respectively of the first stage of the latch 72. A coincidence output signal 82 assumes low level when the output signals Q_A, Q_B, Q_C of

the binary counter 80 become equal to the output signals of A_1, B_1, C_1 of the latch 72. The coincidence output signal 82 causes a data terminal D of a D-type flip-flop 84 to assume high level through a NAND gate 83. Since the second grey scale control clock CLK2 is connected to the clock terminal of the flip-flop 84, an output signal a_1 of the first unit which is the output of the flip-flop 84 assumes low level in response to fall of the second grey scale control clock CLK2. The output signal a_1 of the first unit is connected to an input of the NAND gate 83 and, hence, maintains low level even when the level of the coincidence output signal 82 returns to high level.

Thereafter, the flip-flop 84 is cleared by the horizontal synchronising signal Hs, and the output signal a_1 of the first unit assumes high level.

At the same time, the binary counter 80 is re-set. During the period for which the output signal a_1 of the first unit assumes high level, a selective waveform is applied to the panel 75 through an X bit signal electrode driver 74 shown in Figure 7.

The time chart of Figure 11 illustrates the operation of the grey scale controller 73 in the case where the 3-bit grey scale data is as follows:

$D_2 = 0$ .... MSB
$D_1 = 0$
$D_0 = 1$

0 .... low level
1 .... high level

In this case the first stage of the latch 72 produces the output:

$C_1 = 0$
$B_1 = 0$
$A_1 = 1$

whereby the coincidence output signal 82 assumes high level at a moment when the first grey scale control clock CLK1 is 4.

The output signal a_1 of the first unit of the grey scale controller 3 assumes low level at a moment when the first grey scale control signal CLK1-4 falls, and this condition is maintained until the next horizontal synchronising signal Hs is input.

Output signals a_1 to a_x of the grey scale controller 73 drive signal electrodes S_1 to S_x of the panel 75 of Figure 7 through the signal electrode driver 74.

Electrodes C_1 to C_y on the scanning side of the panel 75 are driven by a voltage averaging method that is usually employed for driving the liquid crystal cells, by a Y bit shift register 76 and a Y bit scanning electrode driver 77. A signal FRM is a frame signal which indicates the start of a frame, and DF denotes a liquid crystal AC inverting signal.

A power supply 78 generates a selective voltage or a non-selective voltage that will be applied to the signal electrode driver 74 and to the scanning electrode driver 77. A drive waveform applied to the panel 75 is shown in Figure 6, wherein the ON portion represents a grey scale portion by pulse-width modulation.

Figure 12 illustrates another embodiment of an electro-optical modulator according to the present invention. In Figure 12, SBE cells are arranged in the form of an X x Y dot matrix SBE panel 125 and are driven by pulse-width modulation using 4-bit grey scale display of 8 grades, 4-bit grey scale data D_3 to D_0 being input in the form of binary codes.

As for the relationship between the reflectivity of the panel 125 and the effective voltage, the gradient

of the reflectivity varies at every point of the effective voltage as shown in Figure 10. Therefore, if the grey scale display is effected by simply changing the effective voltage, it is difficult to obtain uniform grey scale display characteristics. Therefore, the effective voltage must be so changed that the reflectivity varies uniformly over a range from 100% to 0% reflectivity. In Figure 14, the reflectivity is plotted in eight steps so that optimum grey scale display characteristics are obtained.

In a grey scale controller 123 the grey scale data D_3 to D_0 of 4-bits is converted into pulse widths of selected waveforms of the panel 125.

The grey scale data D_3 to D_0 is converted as regards their codes by a code conversion circuit 129 based upon the relationship of the reflectivity of the panel 125 and the effective voltage shown in Figure 10.

With reference to the following Table, when the input codes are, for instance, 0H to 3H (hexadecimal notation), the output code is OH which corresponds to 100% of reflectivity of Figure 10.

TABLE OF CODE CONVERSION

	Input code D3	D2	D1	D0	Output code DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0	0	1	0	0
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
A	1	0	1	0	1	0	1	0
B	1	0	1	1	1	0	1	1
C	1	1	0	0	1	1	1	1
D	1	1	0	1				
E	1	1	1	0				
F	1	1	1	1				

When the input codes are from 4H to 6H, the same output code 4H is generated. This corresponds to a point at which the reflectivity has dropped by 1/7 from 100% of reflectivity in Figure 10.

The Table illustrates the conversion in detail. The circuit is constituted by a PLA (programmable logic array). Black circles represent connection points of AND-ROM regions. Open circles represent low level connection points of OR-ROM regions. If now the input code is 5H, the AND-ROM of the third column becomes active to generate OR-ROM data 4H.

The 4-bit grey scale data DB_3 to DB_0 of Figure 12 after conversion by the code conversion circuit 129 is shifted in an X x 4-bit shift register 121 in synchronism with a shift clock CP.

An output 01 of the shift register 121 is latched by an X x 4-bit latch 122 that has X x 4-bit structure, when a horizontal synchronising signal Hs falls. An output 02 of the latch 122 serves as an input signal to the grey scale controller 123 which is the same as shown in Figure 4.

The time chart of Figure 15 illustrates the relationship between the horizontal synchronising signal Hs and the grey scale control clocks CLK. That is, 16 grey scale control clocks CLK are input within one period of the horizontal synchronising signal Hs with the rise thereof as a starting point.

Figure 15 illustates the case where the 4-bit grey scale data is as follows:

$D_3 = 0$ .... MSB
$D_2 = 1$
$D_1 = 1$
$D_0 = 0$

0 .... low level
1 .... high level

In this case, the first stage of the latch 122 produces the output:

$D_1 = 0$
$C_1 = 1$
$B_1 = 0$
$A_1 = 0$

whereby the coincidence output signal 42 assumes high level at a moment when the grey scale control clock CLK is 0, and assumes low level at a moment when the grey scale control clock CLK is 4.

The output signal a_1 of the first stage of the grey scale controller 123 assumes low level at the moment when the grey scale control signal CLK-4 falls, and this condition is maintained until the next horizontal synchronising signal Hs is input.

In the time chart of Figure 14, the period in which the output signal a_1 of the first stage of the grey scale control circuit 123 assumes the high level (ON) serves as a selective period.

The output signals a_1 to a_x of the grey scale controller 123 drive signal electrodes S_1 to S_x of the panel 125 of Figure 12 through an X bit signal electrode driver 124.

Electrodes C_1 to C_y on the scanning side of the panel are driven by a voltage averaging method that is usually employed for driving liquid crystal cells, and by a Y bit shift register 126 and a Y bit scanning electrode driver 127. A signal FRM is a frame signal

which indicates the start of the frame, and DF denotes a liquid crystal AC inverting signal.

A power supply 128 generates a selective voltage or a non-selective voltage that will be applied to the signal electrode driver 124 and to the scanning electrode driver 127. A drive waveform applied to the panel 125 is shown in Figure 6, wherein the ON portion of the voltage across the panel corresponds to the ON portion of the output signal a_1 in the time chart of Figure 14.

As will be appreciated from the foregoing description, the code is so converted so that the grey scale data that determines the grey scale is adapted to the reflectivity characteristics of the SBE cells, and the pulse-width modulation is effected by the grey scale controller 123, in order to obtain optimum grey scale display characteristics.

The panel 125 arranged in the form of a dot matrix is adapted to the reflectivity characteristics of the SBE cells to realise an optimum grey scale display. It is, therefore, possible to obtain an electro-optical modulator which displays data maintaining high display quality. Further, when the SBE cells are to be used to form an optical shutter, such as an electronic curtain or a shutter for a printer, the shutter can be provided with a grey scale function.

CLAIMS

1. An electro-optical modulator comprising: a dot matrix liquid crystal panel (3) using supertwisted birefringence effect, the panel having a plurality of scanning electrodes and a plurality of signal electrodes; a scanning electrode driving means;, and a signal electrode driving means having a grey scale function.

2. An electro-optical modulator as claimed in claim 1 in which the gray scale function is, in operation, performed by frequency modulation.

3. An electro-optical modulator as claimed in claim 1 in which the grey scale function is, in operation, performed by pulse width modulation.

4. An electro-optical modulator as claimed in claim 3 in which the signal electrode driving means includes means for changing grey scale display data to a signal with a desired pulse width to be applied to the signal electrodes.

5. An electro-optical modulator as claimed in claim 4 in which, in operation, the grey scale display data is changed to a signal with a desired pulse width which has one or more units, one unit being equal to a period of a grey scale control clock.

6. An electro-optical modulator as claimed in any of claims 3 to 5 having a plurality of grades of grey scale function, each pulse width corresponding to each of the grades of the grey scale being set so that the change of the grades of grey scale to the change of the grades of the pulse width is substantially constant.

7. An electro-optical modulator as claimed in claim 6 in which, in operation, the pulse width is changed by changing the period of the grey scale control

clock signal.

8. An electro-optical modulator as claimed in any preceding claim in which the signal electrode driving means comprises a shift register for receiving and shifting grey scale data, a latch for latching the output of the shift register, a grey scale controller for changing the output of the latch to a signal having a desired selective time width according to the content of the output of the latch, the desired selective time width having one or more units one of which is equal to a period of a grey scale control clock, and a signal electrode driver for changing the output of the grey scale controller to a liquid crystal driving signal.

9. An electro-optical modulator as claimed in claim 8 in which the grey scale controller comprises a counter for counting the grey scale control clock, and a plurality of circuit units each of which has a coincidence circuit for examining coincidence between the output signal of said counter and the output signal of the latch, and a latching circuit for latching the output of the coincidence circuit synchronising with the grey scale control clock.

10. An electro-optical modulator as claimed in claim 9 in which the number of circuit units is equal to that of signal electrodes of the panel.

11. An electro-optical modulator as claimed in claim 4 or any of claims 5 to 10 when dependent thereon in which the grey scale display data is 2, 3 or 4 bits.

12. An electro-optical modulator as claimed in any preceding claim including a code conversion circuit for converting grey scale data to codes so as to obtain optimum grey scale.

13. An electro-optical modulator substantially as described with reference to and as shown in the

accompanying drawings.

14. Any novel integer or step or combination of integers or steps, hereinbefore described and/or as shown in the accompanying drawings, irrespective of whether the present claim is within the scope of or relates to the same or a different invention from that of, the preceding claims.

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